FIG.1

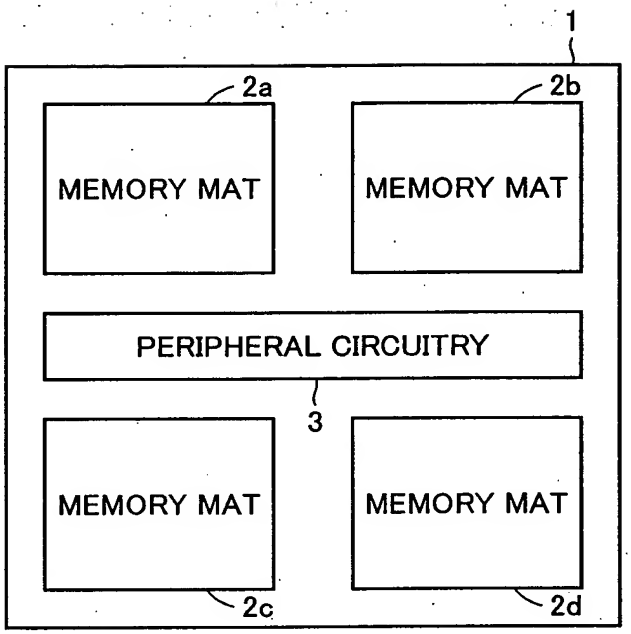

1
2a
2b
MEMORY MAT
MEMORY MAT
PERIPHERAL CIRCUITRY
3
MEMORY MAT
MEMORY MAT
2c
2d

FIG.2

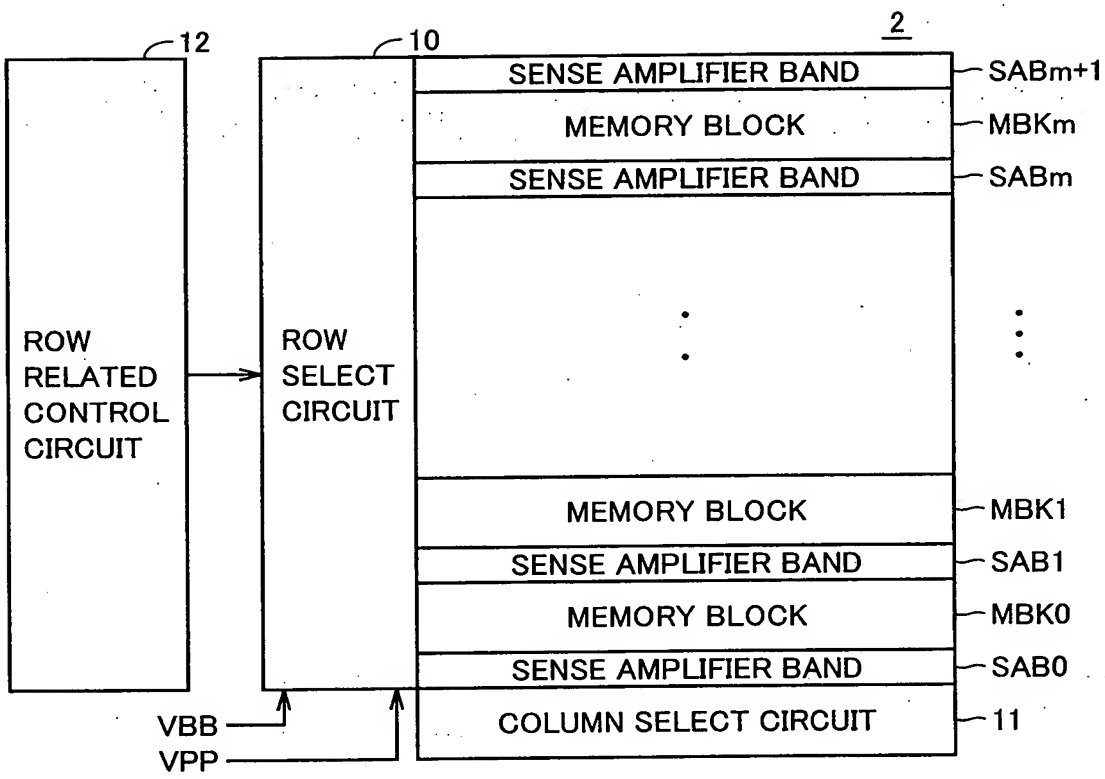

12
10
2
ROW
RELATED
CONTROL
CIRCUIT
ROW
SELECT
CIRCUIT
SENSE AMPLIFIER BAND
SABm+1
MEMORY BLOCK
MBKm
SENSE AMPLIFIER BAND
SABm
MEMORY BLOCK
MBK1
SENSE AMPLIFIER BAND
SAB1
MEMORY BLOCK
MBK0
SENSE AMPLIFIER BAND
SAB0
COLUMN SELECT CIRCUIT
11
VBB
VPP

FIG.3

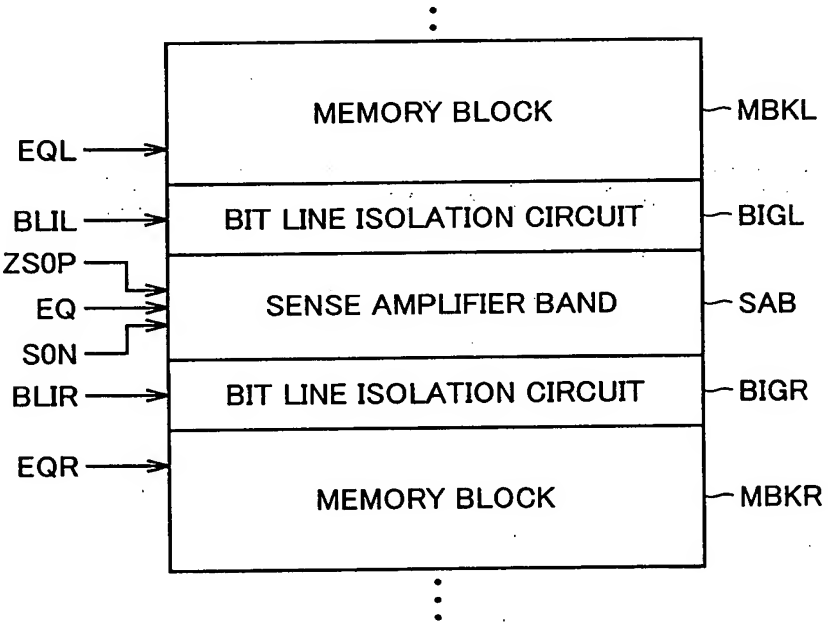

MEMORY BLOCK
MBKL
EQL
BLIL
BIT LINE ISOLATION CIRCUIT
BIGL
ZS0P
EQ
S0N
SENSE AMPLIFIER BAND
SAB
BLIR
BIT LINE ISOLATION CIRCUIT
BIGR
EQR
MEMORY BLOCK
MBKR

FIG.4

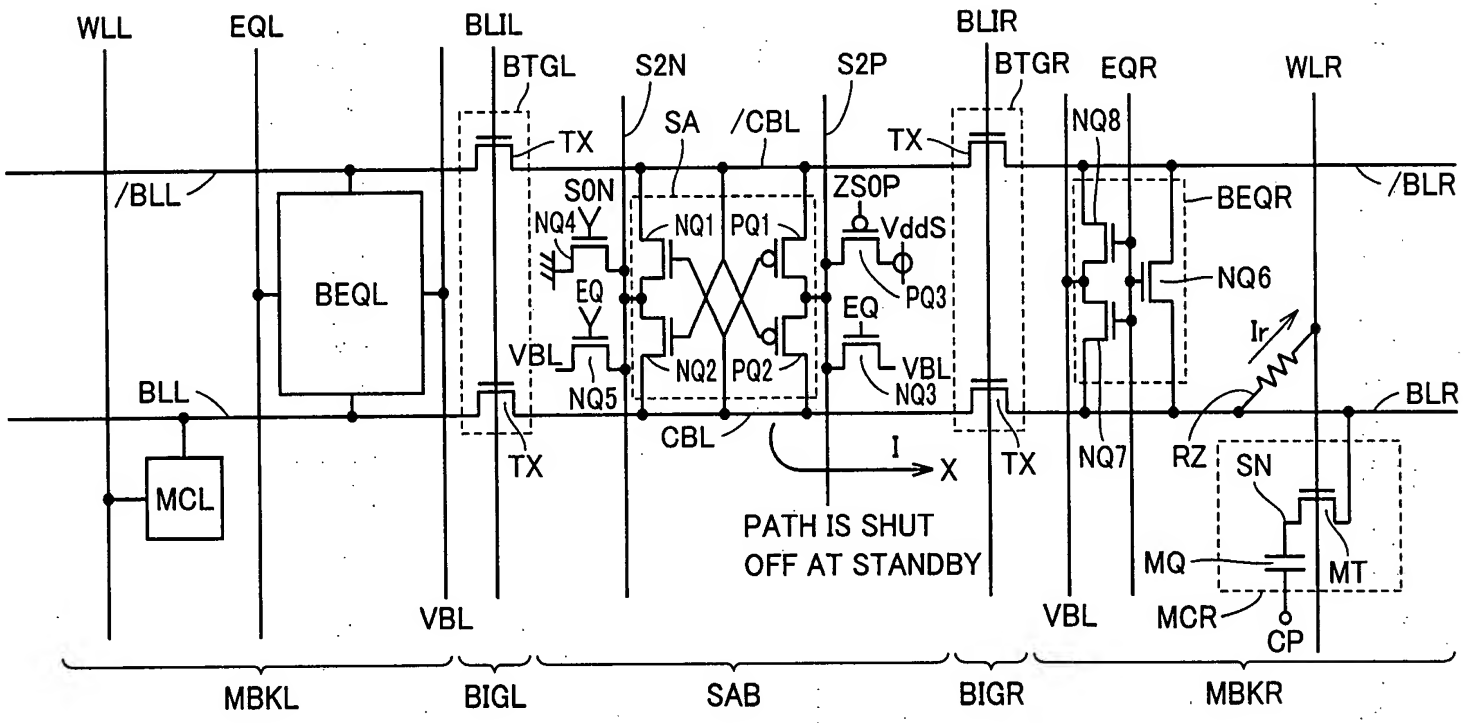

WLL
EQL
BLIL
BTGL
S2N
S2P
BLIR
BTGR
EQR
WLR
TX
SA
/CBL
NQ8
/BLL
S0N
ZS0P
BEQR
/BLR
NQ4
NQ1
PQ1
VddS
BEQL
EQ
PQ3
NQ6
EQ
Ir
VBL
NQ2
PQ2
VBL
BLL
NQ5
NQ3
BLR
CBL
I
X
TX
TX
NQ7
RZ
SN
MCL
PATH IS SHUT
OFF AT STANDBY
MQ
MT
VBL
VBL
MCR
CP
MBKL
BIGL
SAB
BIGR
MBKR

FIG.5

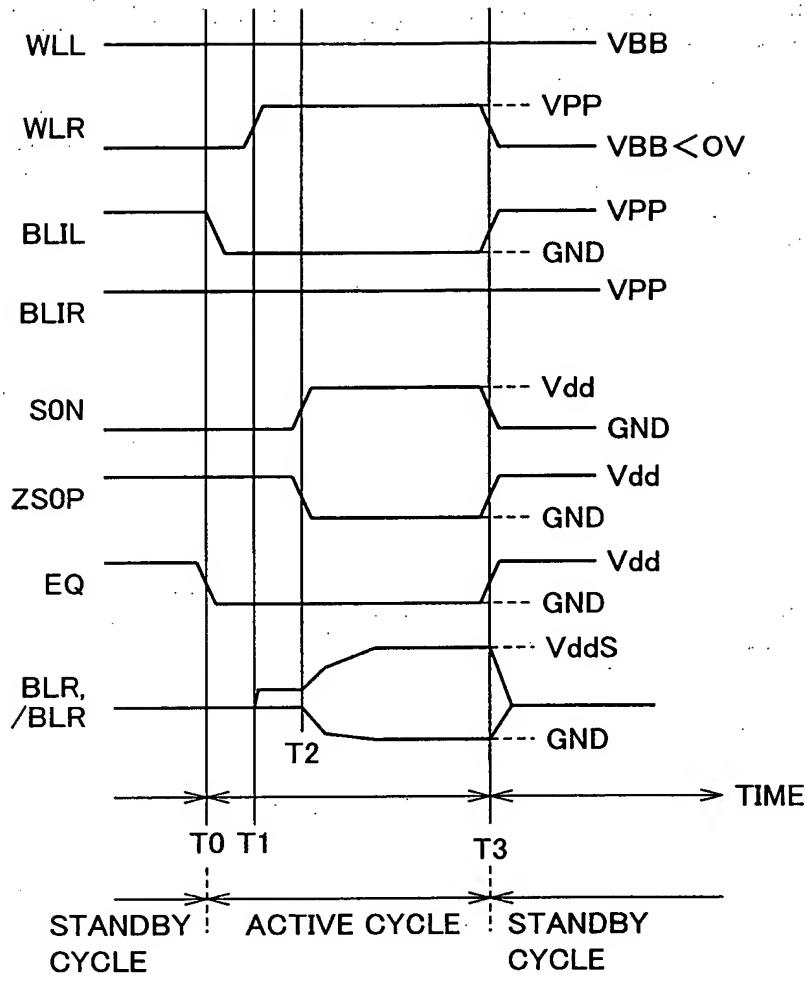

WLL
VBB
WLR
VPP
VBB<OV
BLIL
VPP
GND
BLIR
VPP
SON
Vdd
GND
ZSOP
Vdd
GND
EQ
Vdd
GND
VddS
BLR,
/BLR
GND
T2
TIME
T0 T1
T3
STANDBY
CYCLE
ACTIVE CYCLE
STANDBY
CYCLE

FIG.6

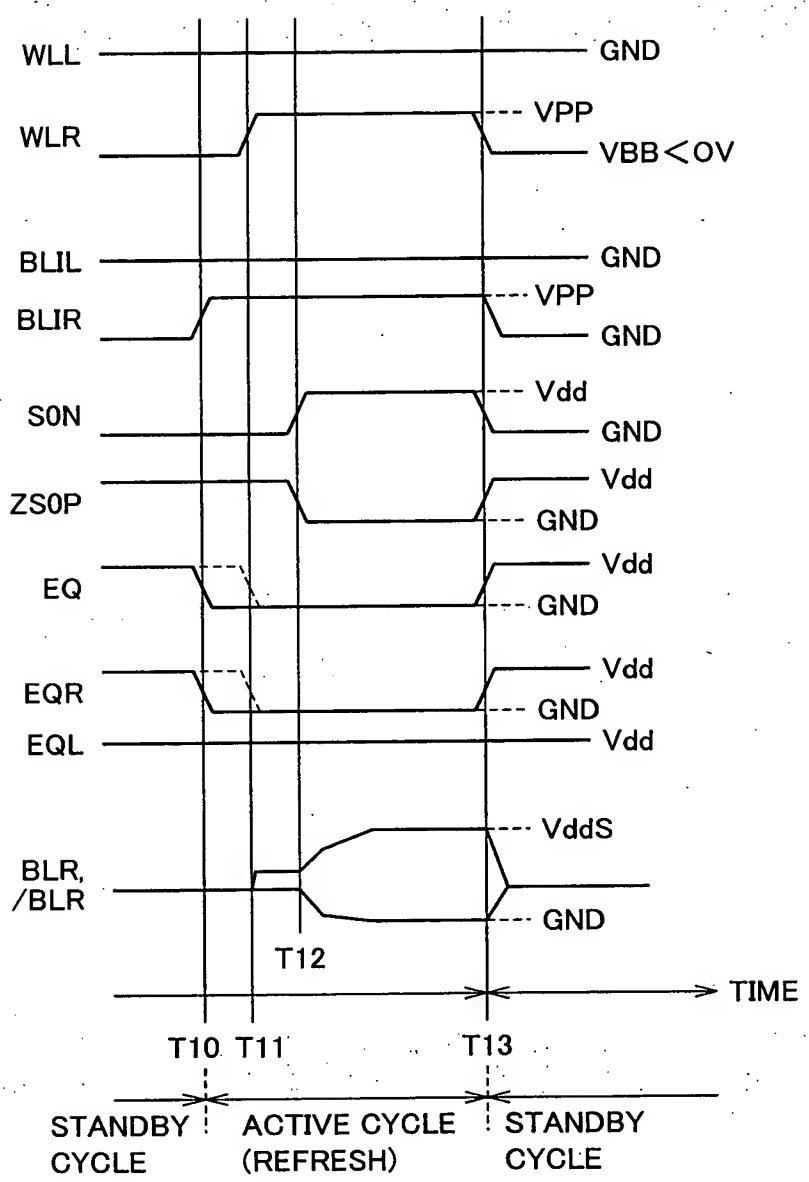

WLL
GND
WLR
VPP
VBB<OV
BLIL
GND
BLIR
VPP
GND
SON
Vdd
GND
ZSOP
Vdd
GND
EQ
Vdd
GND
EQR
Vdd
GND
EQL
Vdd
BLR,
/BLR
VddS
GND
T12
TIME
T10
T11
T13
STANDBY CYCLE
ACTIVE CYCLE (REFRESH)
STANDBY CYCLE

FIG.7

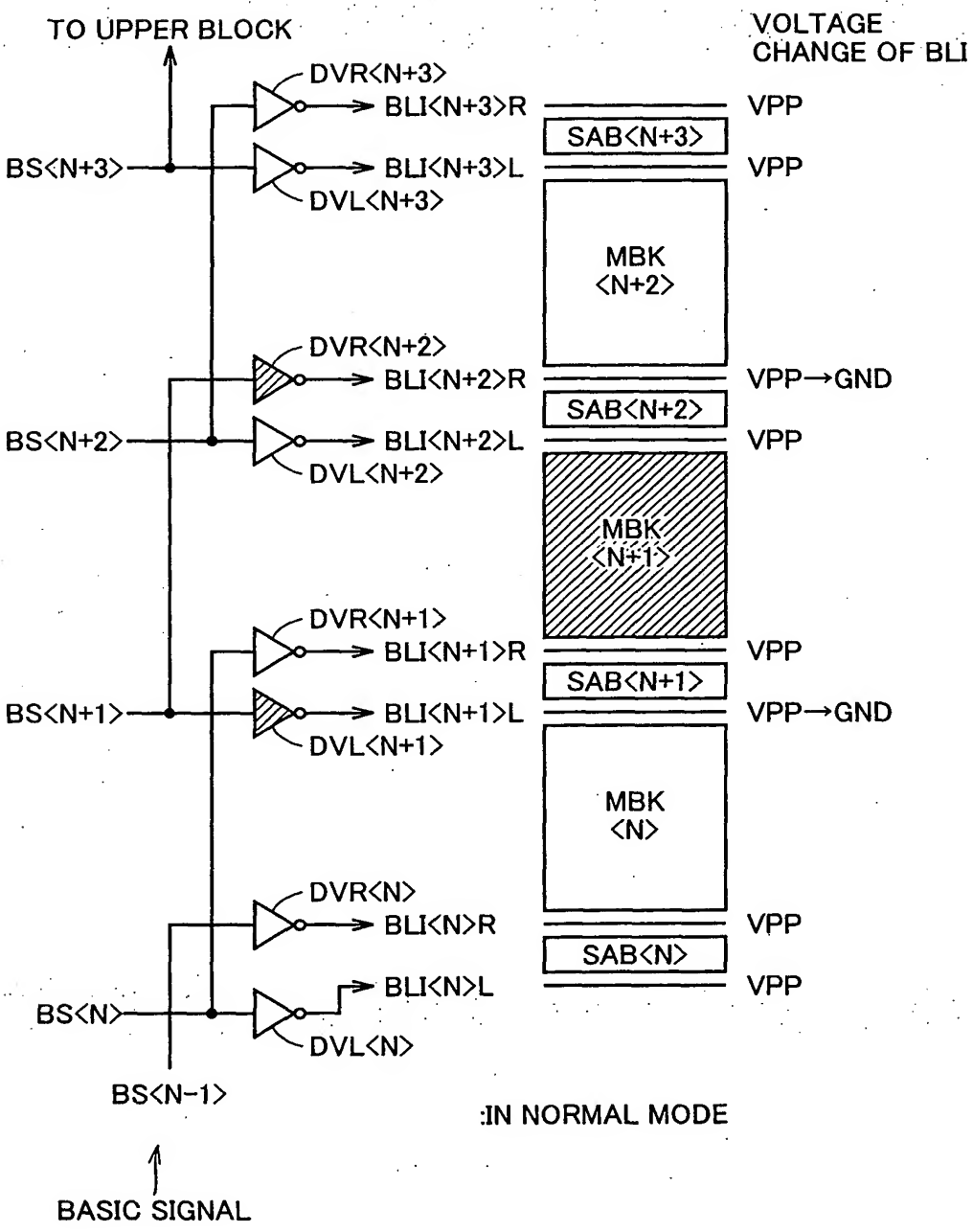

TO UPPER BLOCK
VOLTAGE CHANGE OF BLI
DVR<N+3>
BLI<N+3>R
VPP
SAB<N+3>
BS<N+3>
BLI<N+3>L
VPP
DVL<N+3>
MBK <N+2>
DVR<N+2>
BLI<N+2>R
VPP→GND
SAB<N+2>
BS<N+2>
BLI<N+2>L
VPP
DVL<N+2>
MBK <N+1>
DVR<N+1>
BLI<N+1>R
VPP
SAB<N+1>
BS<N+1>
BLI<N+1>L
VPP→GND
DVL<N+1>
MBK <N>
DVR<N>
BLI<N>R
VPP
SAB<N>
BLI<N>L
VPP
BS<N>
DVL<N>
BS<N-1>
:IN NORMAL MODE
BASIC SIGNAL

FIG.8

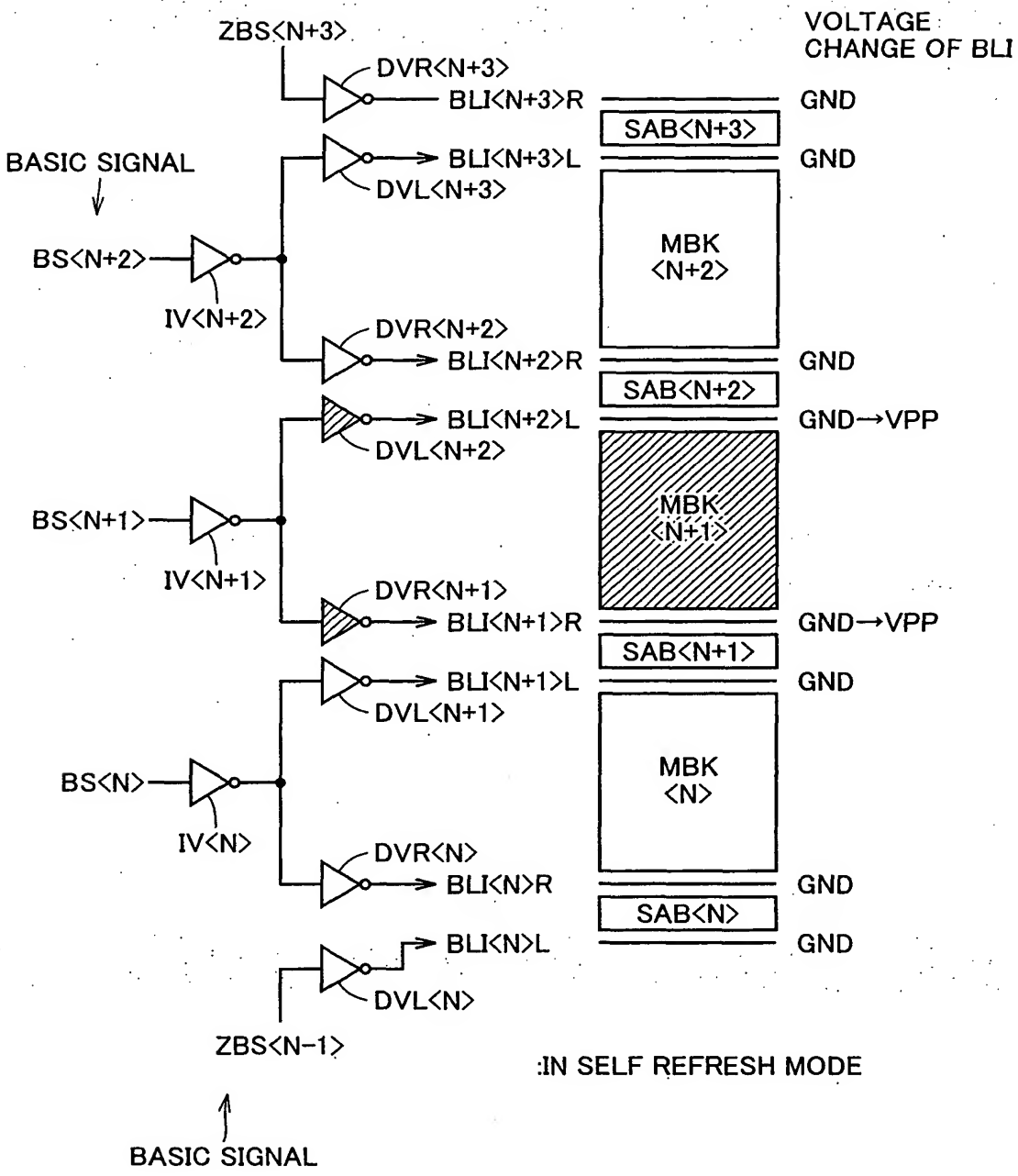

ZBS<N+3>
VOLTAGE CHANGE OF BLI
DVR<N+3>
BLI<N+3>R
GND
SAB<N+3>
BASIC SIGNAL
BLI<N+3>L
GND
DVL<N+3>
MBK <N+2>
BS<N+2>
IV<N+2>
DVR<N+2>
BLI<N+2>R
GND
SAB<N+2>
BLI<N+2>L
GND→VPP
DVL<N+2>
MBK <N+1>
BS<N+1>
IV<N+1>
DVR<N+1>
BLI<N+1>R
GND→VPP
SAB<N+1>
BLI<N+1>L
GND
DVL<N+1>
MBK <N>
BS<N>
IV<N>
DVR<N>
BLI<N>R
GND
SAB<N>
BLI<N>L
GND
DVL<N>
ZBS<N-1>
:IN SELF REFRESH MODE
BASIC SIGNAL

FIG.9

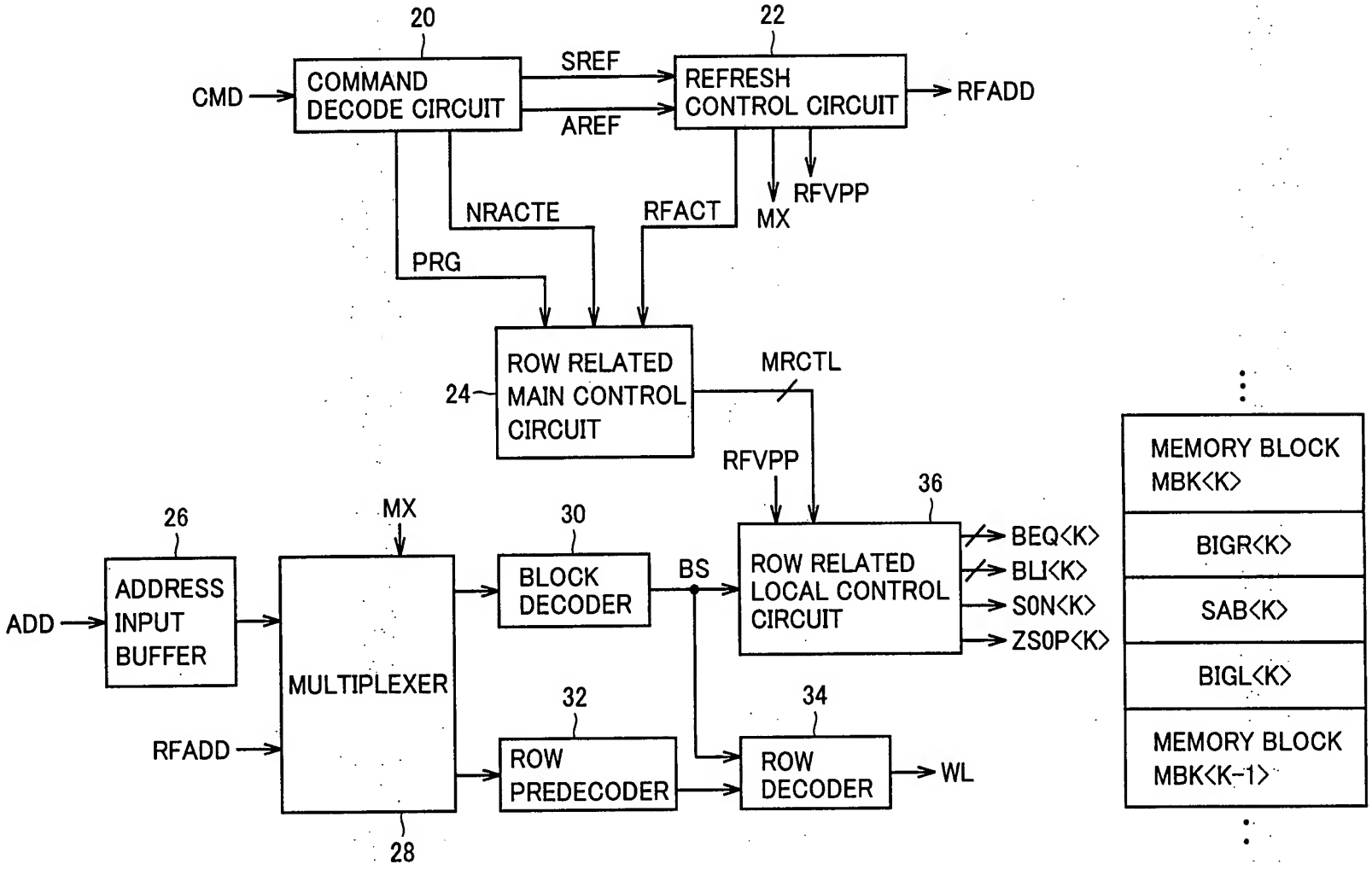

20
22
CMD
COMMAND DECODE CIRCUIT
SREF
AREF
REFRESH CONTROL CIRCUIT
RFADD
NRACTE
RFACT
MX
RFVPP
PRG
ROW RELATED MAIN CONTROL CIRCUIT
24
MRCTL
RFVPP
36
26
MX
30
ADD
ADDRESS INPUT BUFFER
MULTIPLEXER
BLOCK DECODER
BS
ROW RELATED LOCAL CONTROL CIRCUIT
BEQ<K>
BLI<K>
S0N<K>
ZS0P<K>
RFADD
32
34
ROW PREDECODER
ROW DECODER
WL
28
MEMORY BLOCK MBK<K>
BIGR<K>
SAB<K>
BIGL<K>
MEMORY BLOCK MBK<K-1>

FIG.10

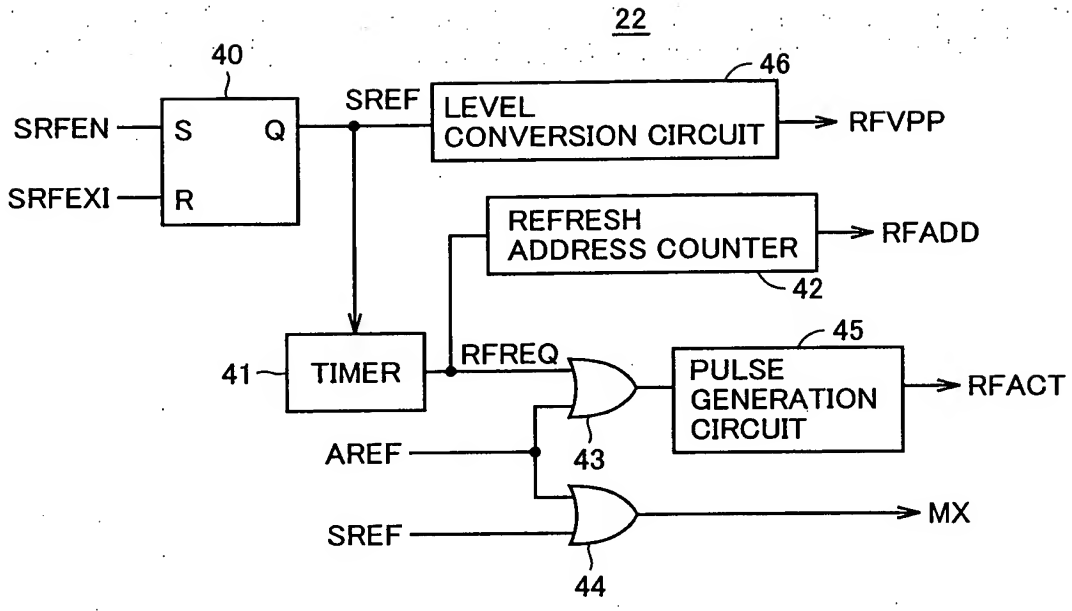

22
40
SREF
46
SRFEN
S
Q
LEVEL CONVERSION CIRCUIT
RFVPP
SRFEXI
R
REFRESH ADDRESS COUNTER
RFADD
42
45
41
TIMER
RFREQ
PULSE GENERATION CIRCUIT
RFACT
AREF
43
MX
SREF
44

FIG.11

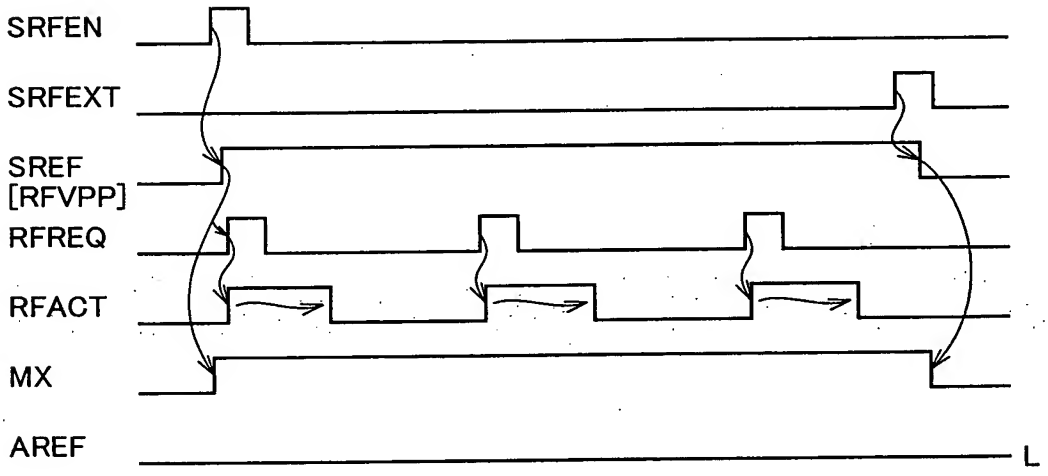

SRFEN
SRFEXT
SREF
[RFVPP]
RFREQ
RFACT
MX
AREF
L

FIG.12

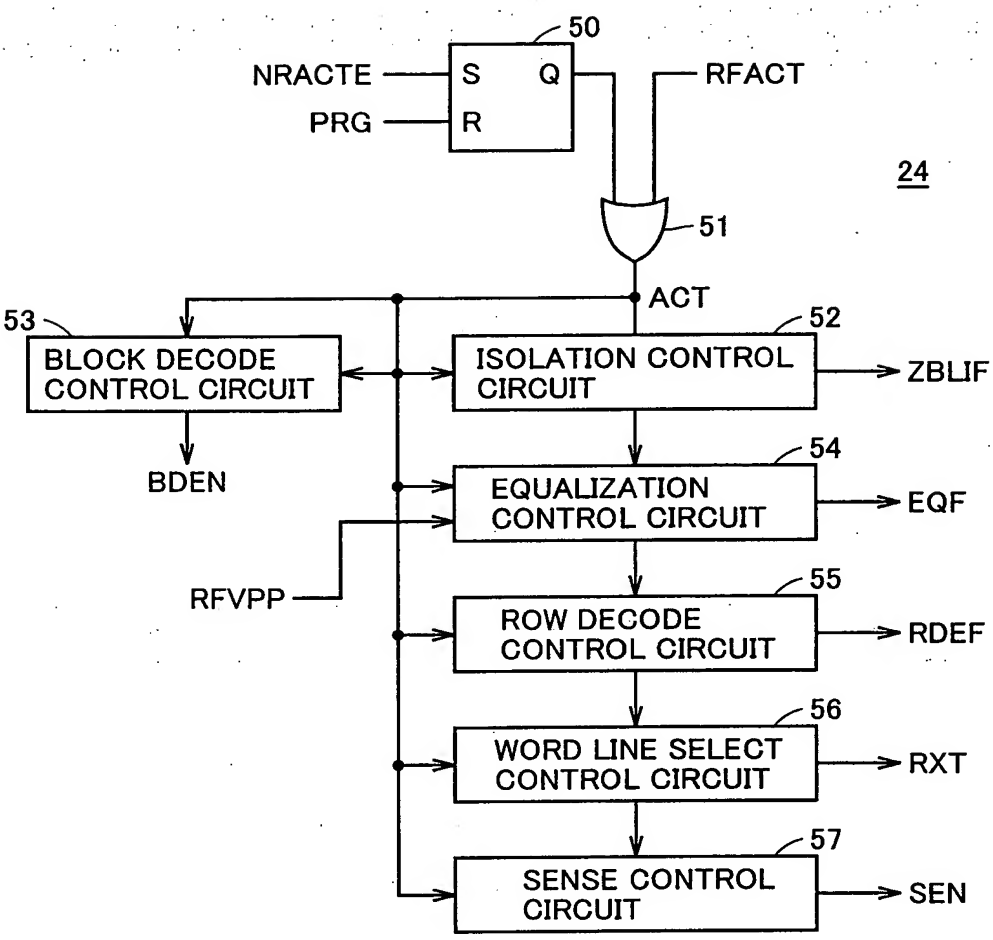

50
NRACTE
S
Q
RFACT
PRG
R
24
51
ACT
53
52
BLOCK DECODE CONTROL CIRCUIT
ISOLATION CONTROL CIRCUIT
ZBLIF
BDEN
54
EQUALIZATION CONTROL CIRCUIT
EQF
RFVPP
55
ROW DECODE CONTROL CIRCUIT
RDEF
56
WORD LINE SELECT CONTROL CIRCUIT
RXT
57
SENSE CONTROL CIRCUIT
SEN

FIG.13

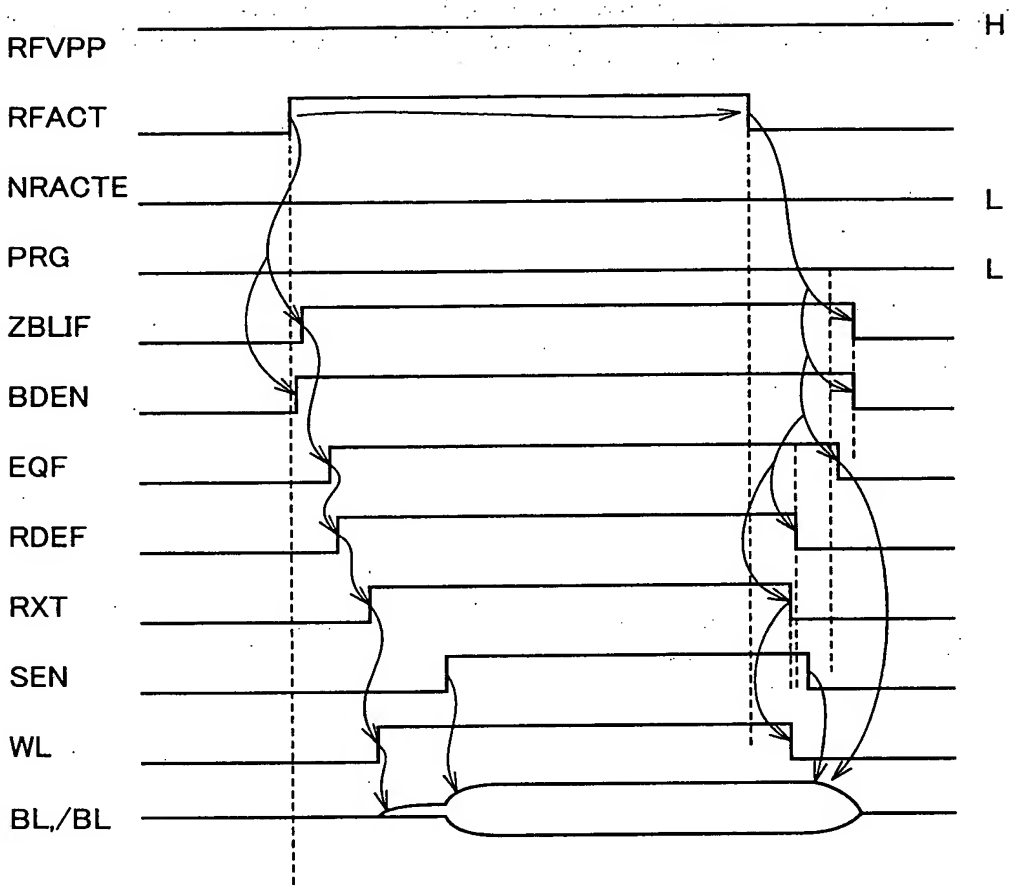

RFVPP
RFACT
NRACTE
PRG
ZBLIF
BDEN
EQF
RDEF
RXT
SEN
WL
BL,/BL
H
L
L

FIG.14

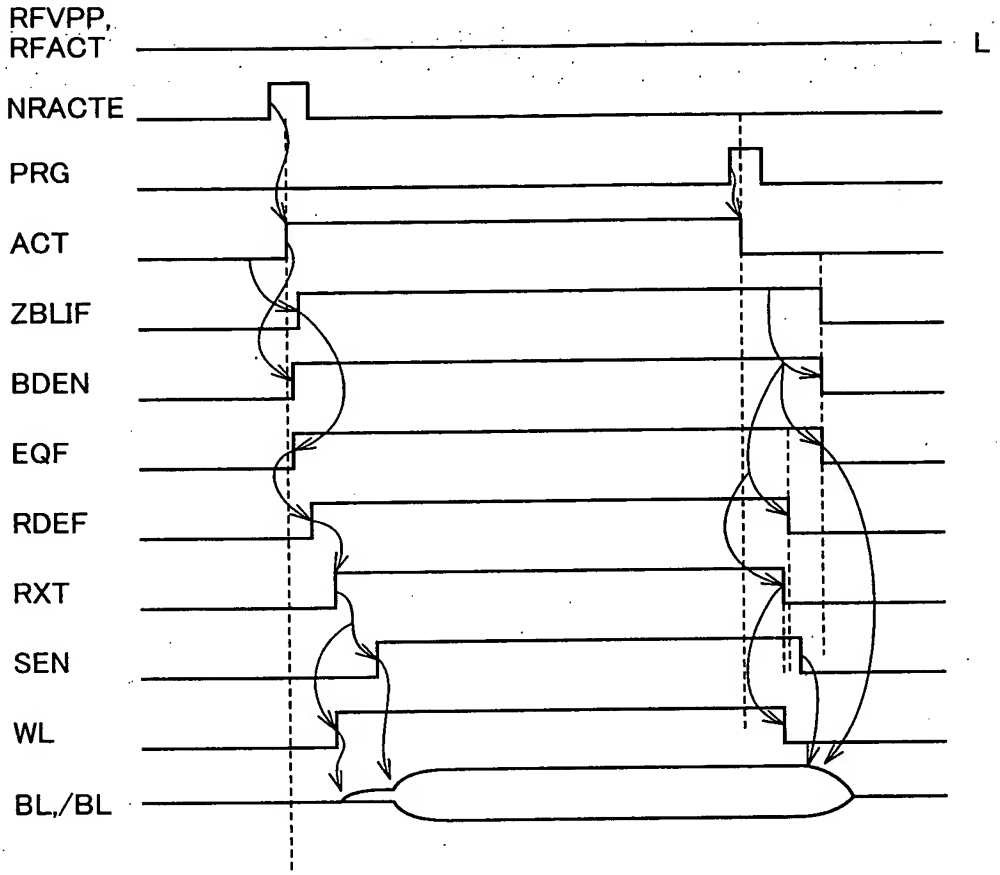

RFVPP,
RFACT
L
NRACTE
PRG
ACT
ZBLIF
BDEN
EQF
RDEF
RXT
SEN
WL
BL,/BL

FIG.15

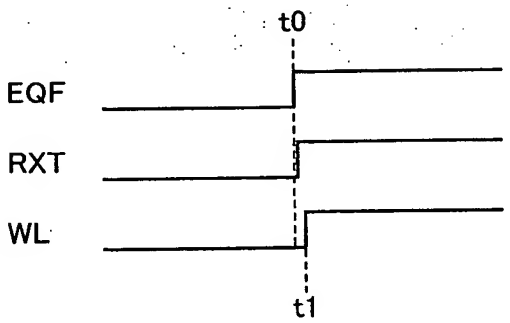

t0
EQF
RXT
WL
t1

FIG.16

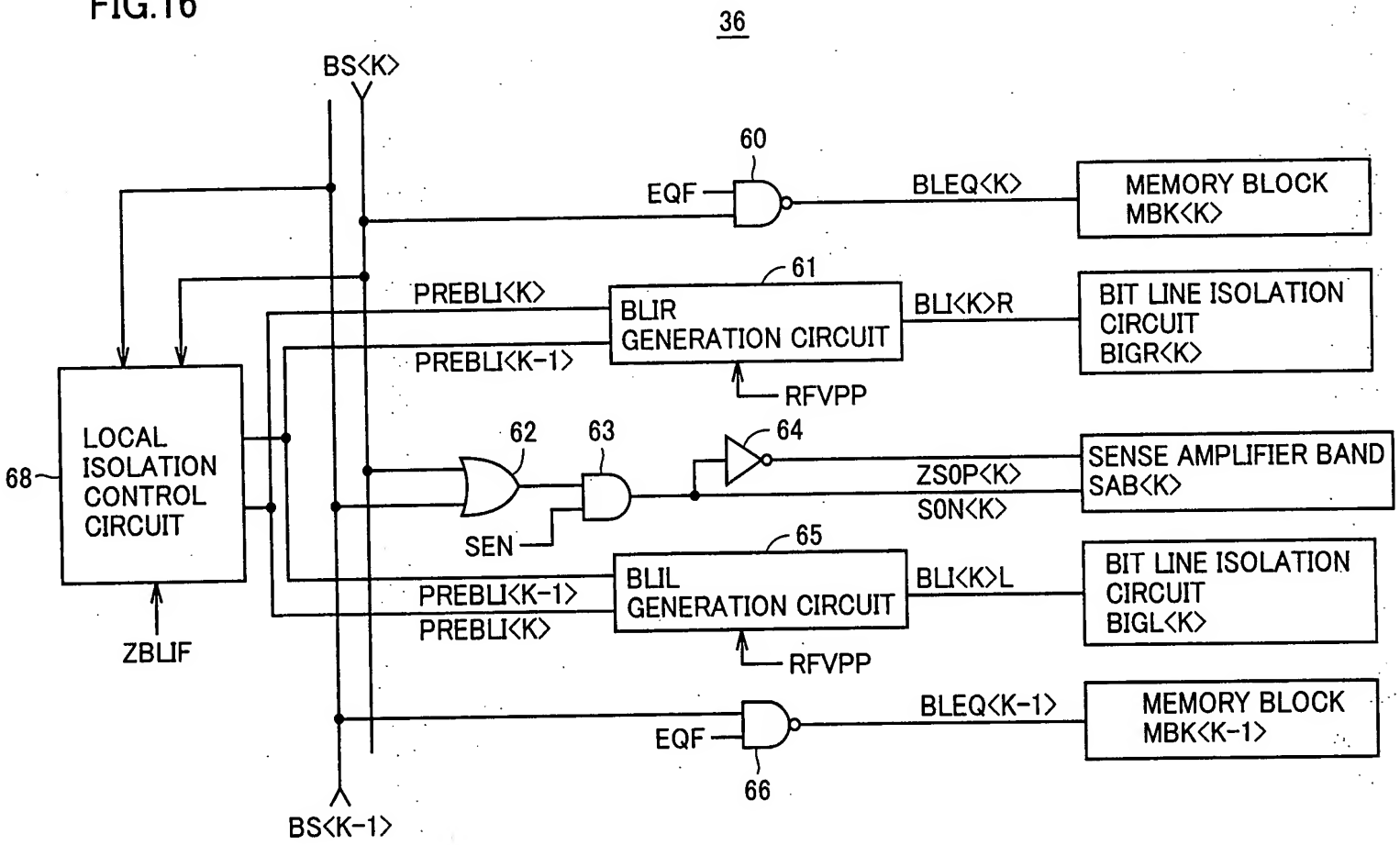

36
BS<K>
60
EQF
BLEQ<K>
MEMORY BLOCK
MBK<K>
61
PREBLI<K>
BLIR
GENERATION CIRCUIT
BLI<K>R
BIT LINE ISOLATION
CIRCUIT
BIGR<K>
PREBLI<K-1>
RFVPP
LOCAL
ISOLATION
CONTROL
CIRCUIT
68
62
63
64
ZS0P<K>
SENSE AMPLIFIER BAND
SAB<K>
S0N<K>
SEN
65
BLIL
GENERATION CIRCUIT
BLI<K>L
BIT LINE ISOLATION
CIRCUIT
BIGL<K>
PREBLI<K-1>
PREBLI<K>
RFVPP
ZBLIF
BLEQ<K-1>
MEMORY BLOCK
MBK<K-1>
EQF
66
BS<K-1>

FIG.17

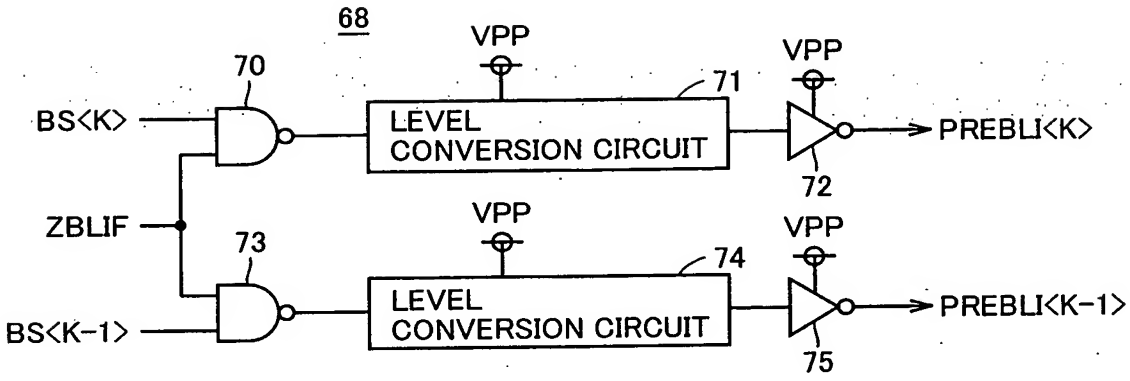


FIG.18

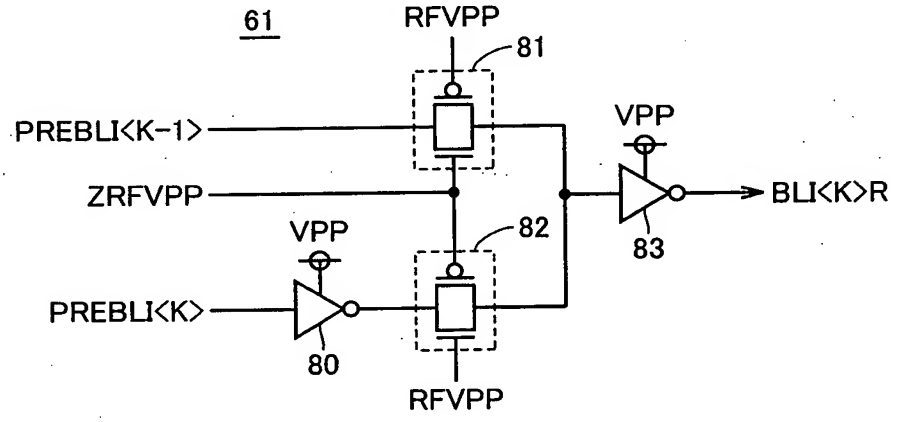


FIG.19

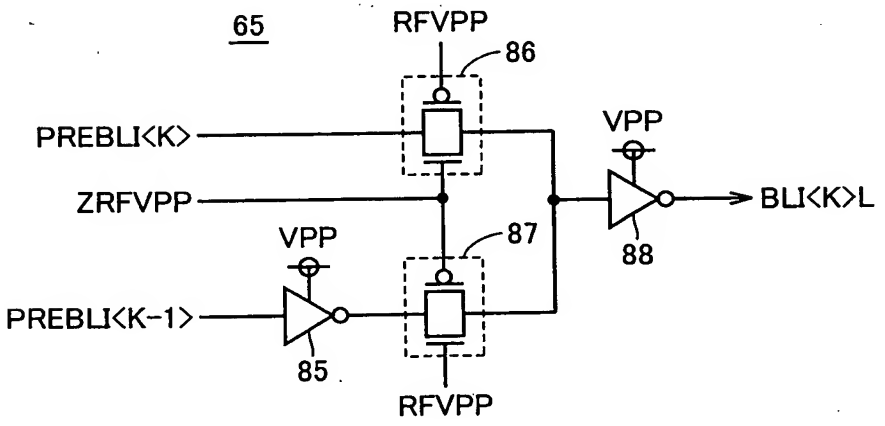


FIG.20

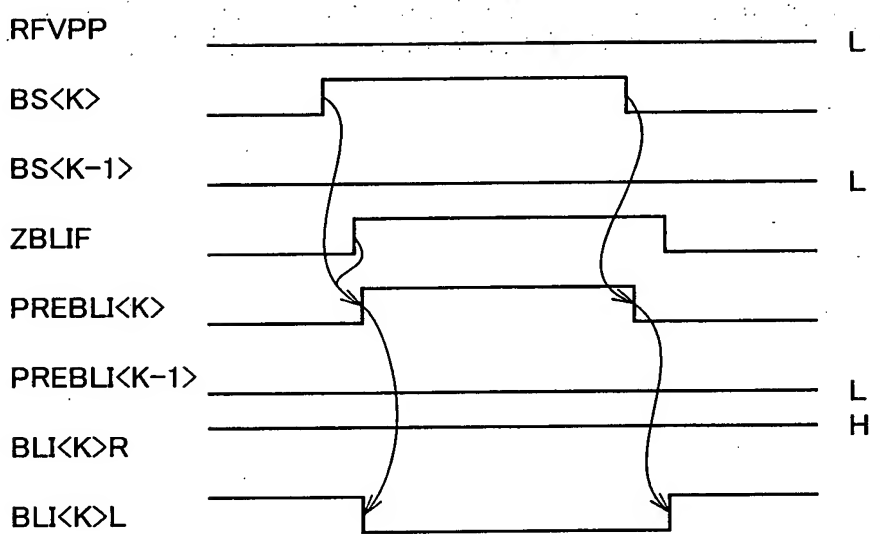

RFVPP
BS<K>
BS<K-1>
ZBLIF
PREBLI<K>
PREBLI<K-1>
BLI<K>R
BLI<K>L
L
L
L
H

FIG.21

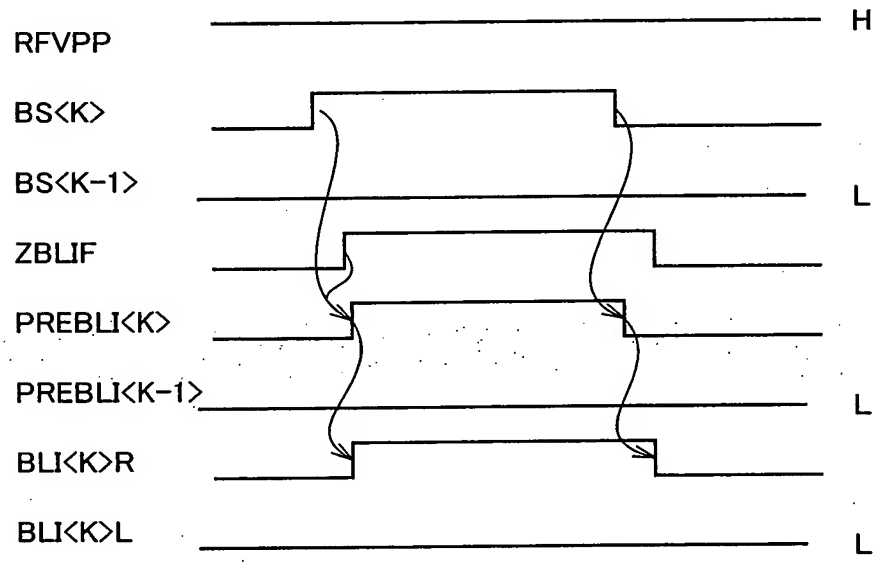

RFVPP
BS<K>
BS<K-1>
ZBLIF
PREBLI<K>
PREBLI<K-1>
BLI<K>R
BLI<K>L
H
L
L
L

FIG.22

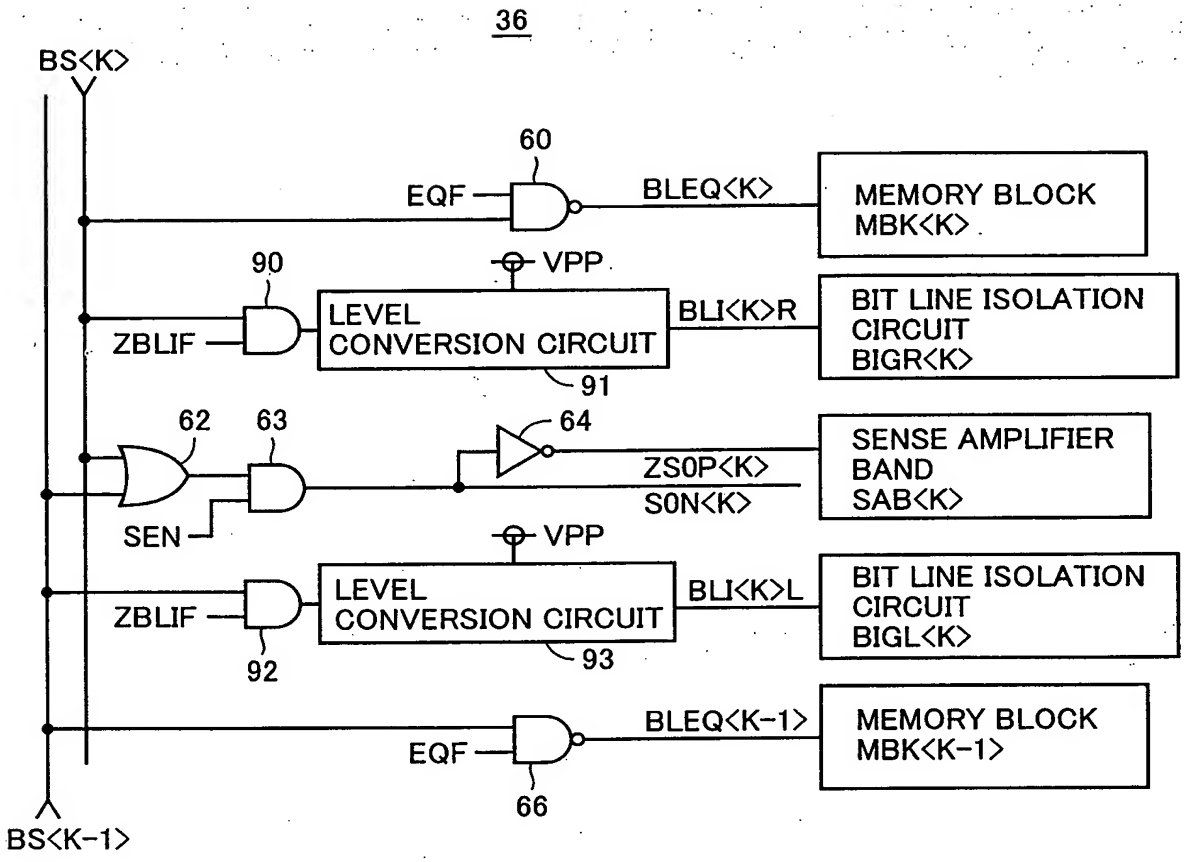

36
BS<K>
60
EQF
BLEQ<K>
MEMORY BLOCK
MBK<K>
90
VPP
ZBLIF
LEVEL
CONVERSION CIRCUIT
BLI<K>R
BIT LINE ISOLATION
CIRCUIT
BIGR<K>
91
62
63
64
SENSE AMPLIFIER
BAND
SAB<K>
ZS0P<K>
S0N<K>
SEN
VPP
ZBLIF
LEVEL
CONVERSION CIRCUIT
BLI<K>L
BIT LINE ISOLATION
CIRCUIT
BIGL<K>
92
93
BLEQ<K-1>
MEMORY BLOCK
MBK<K-1>
EQF
66
BS<K-1>

FIG.23

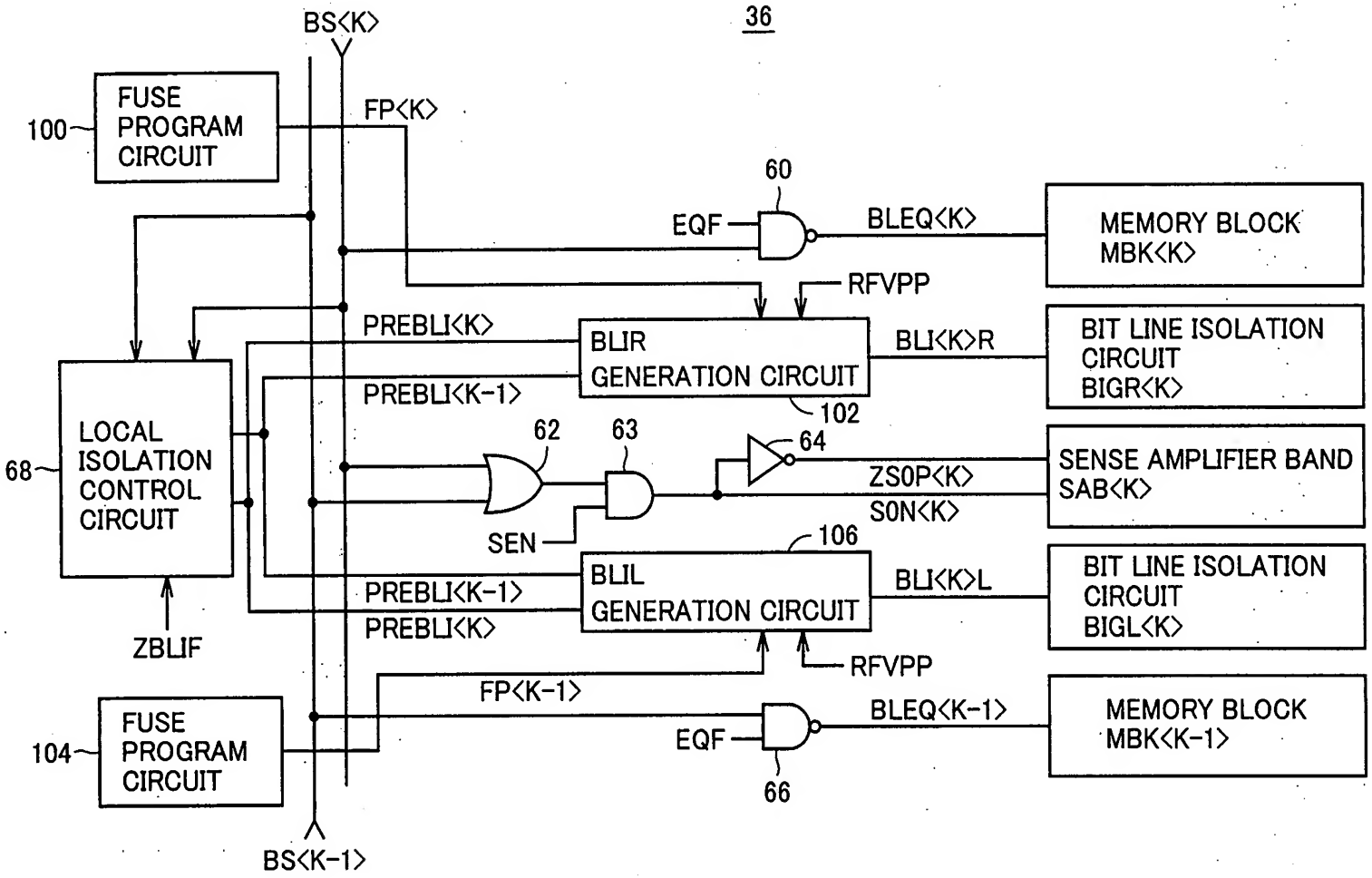

36
BS<K>
FUSE PROGRAM CIRCUIT
100
FP<K>
60
EQF
BLEQ<K>
MEMORY BLOCK MBK<K>
RFVPP
PREBLI<K>
BLIR GENERATION CIRCUIT
BLI<K>R
BIT LINE ISOLATION CIRCUIT BIGR<K>
PREBLI<K-1>
102
LOCAL ISOLATION CONTROL CIRCUIT
68
62
63
64
ZS0P<K>
SENSE AMPLIFIER BAND SAB<K>
S0N<K>
SEN
106
BLIL GENERATION CIRCUIT
BLI<K>L
BIT LINE ISOLATION CIRCUIT BIGL<K>
PREBLI<K-1>
PREBLI<K>
ZBLIF
RFVPP
FP<K-1>
BLEQ<K-1>
MEMORY BLOCK MBK<K-1>
FUSE PROGRAM CIRCUIT
104
EQF
66
BS<K-1>

FIG.24

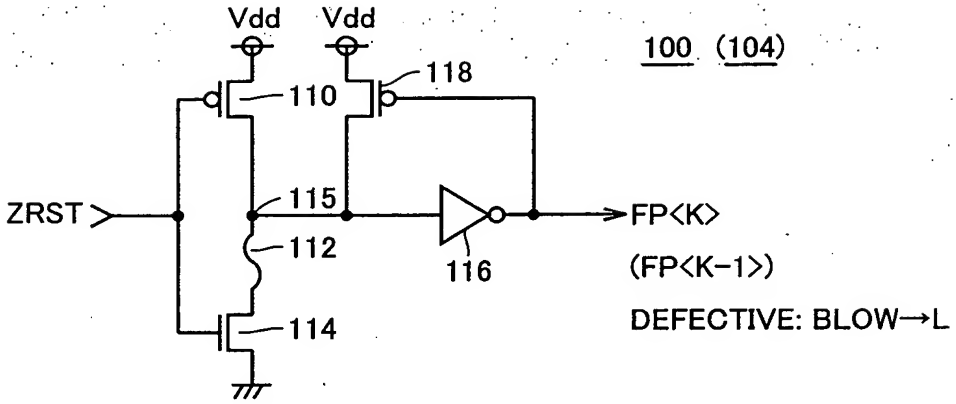

Vdd
Vdd
100 (104)
118
110
ZRST
115
FP<K>
112
116
(FP<K-1>)
114
DEFECTIVE: BLOW→L

FIG.25

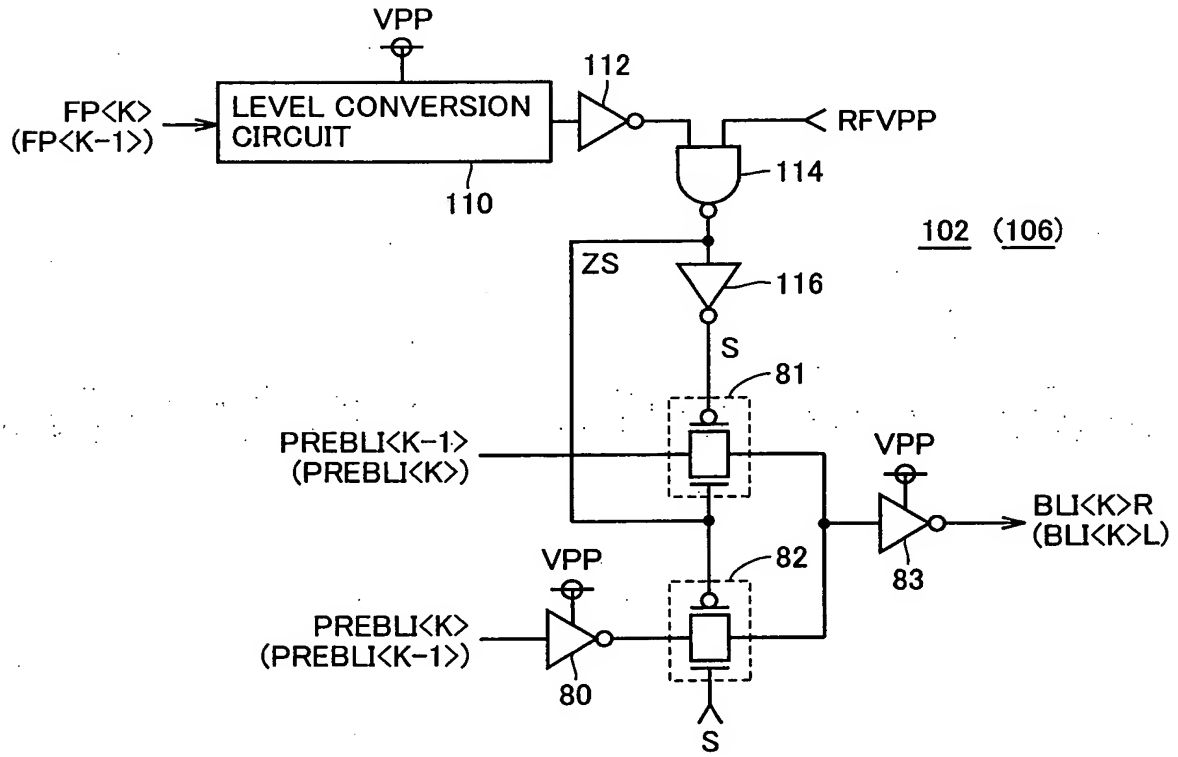
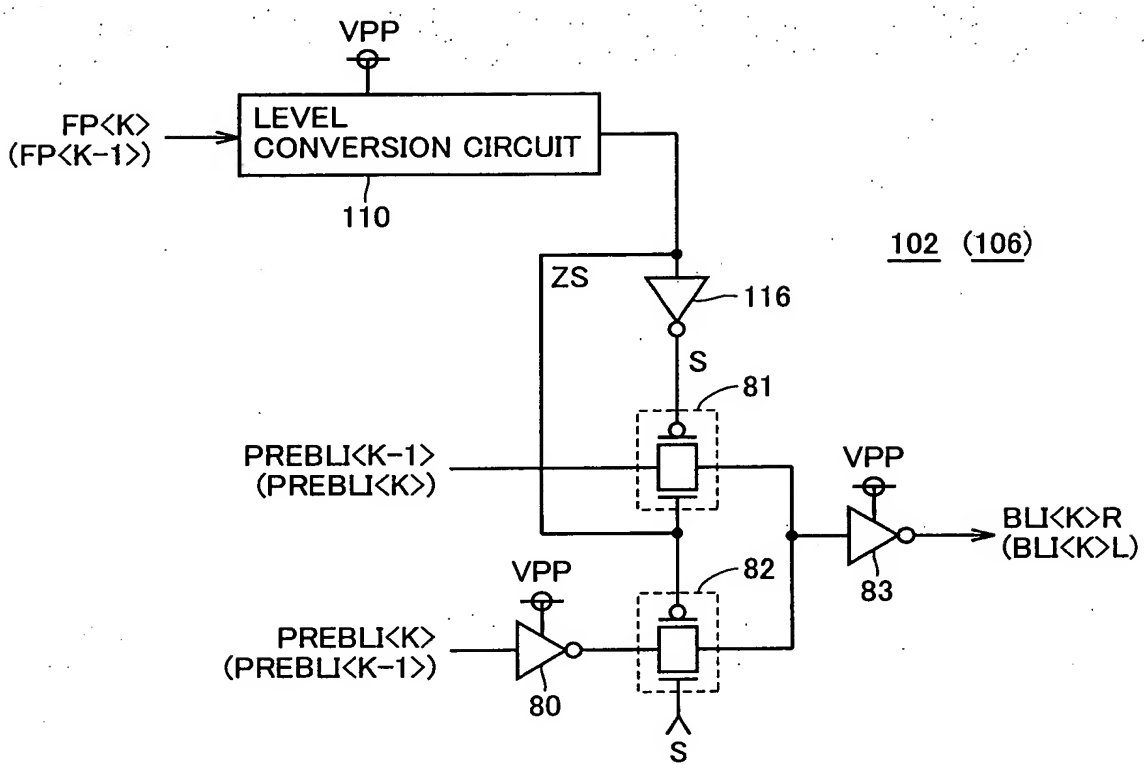

VPP
112
FP<K>
(FP<K-1>)
LEVEL CONVERSION CIRCUIT
RFVPP
110
114
102 (106)
ZS
116
S
81
PREBLI<K-1>
(PREBLI<K>)
VPP
BLI<K>R
(BLI<K>L)
VPP
82
83
PREBLI<K>
(PREBLI<K-1>)
80
S

FIG.26


VPP
FP<K>
(FP<K-1>)
LEVEL
CONVERSION CIRCUIT
110
102 (106)
ZS
116
S
81
PREBLI<K-1>
(PREBLI<K>)
VPP
BLI<K>R
(BLI<K>L)
83
VPP
82
PREBLI<K>
(PREBLI<K-1>)
80
S